What is claimed is:

1. An ESD protection circuit with high substrate-triggering efficiency comprising:

a multi-finger-type device having a plurality of finger gates below which parasitic BJTs are formed, a plurality of finger sources, each of which is an emitter of one of the parasitic BJTs, and at least one finger drain coupled to a pad;

a plurality of voltage drop elements, each of which is coupled between one of the finger sources and a power line to detect a transient current flowing through one of the finger gates; and

a plurality of feedback circuits, each of which is coupled between a base and an emitter respectively of a first and second parasitic BJT, and activates the first BJT to bypass ESD current during an ESD event.

2. The ESD protection circuit as claimed in claim 1, wherein the multi-finger-type device is a multi-finger-type NMOS.

3. The ESD protection circuit as claimed in claim 1, wherein the multi-finger-type device is a multi-finger-type PMOS.

4. The ESD protection circuit as claimed in claim 1, wherein one of the finger gates is coupled to the power line.

5. The ESD protection circuit as claimed in claim 4, wherein one of the finger gates is coupled to the power line through a resistor.

6. The ESD protection circuit as claimed in claim 1, wherein one of the finger gates is coupled to a pre-driver.

7. The ESD protection circuit as claimed in claim 1, wherein the voltage drop elements are resistors.

8. The ESD protection circuit as claimed in claim 7, wherein the resistors are formed by a well of a first conductivity in a substrate of a second conductivity.

9. The ESD protection circuit as claimed in claim 1, wherein the voltage drop elements are inductors.

10. The ESD protection circuit as claimed in claim 1, wherein one of the voltage drop elements is a diode.

11. The ESD protection circuit as claimed in claim 1, wherein one of the voltage drop elements is a series of diodes.

12. The ESD protection circuit as claimed in claim 1, wherein each of the feedback circuits couples the base of the first parasitic BJT to a collector of the second parasitic BJT.

13. The ESD protection circuit as claimed in claim 1, wherein each of the feedback circuits couples the base and a

collector of the first parasitic BJT, and a collector of the second parasitic BJT together.

14. The ESD protection circuit as claimed in claim 1, wherein the multi-finger-type device is a stacked MOS.

15. An ESD protection circuit with high substrate-triggering efficiency formed on a substrate of a second conductivity comprising:

a guard ring of the second conductivity formed on the substrate as a contact region thereof;

a plurality of fingers enclosed by the guard ring, each of which has a finger source formed by a first doping region of a first conductivity, a finger drain formed by a second doping region of the first conductivity and coupled to a pad, a finger gate between the first and second doping region, and a substrate current input node formed by a third doping region of the second conductivity enclosed by the second doping region, wherein the first and second doping region, and the proximate substrate form a parasitic BJT;

a plurality of resistors formed by wells, each of which is coupled between one of the finger sources and a power line; and

internal connection circuits coupling one of the finger sources to one of the substrate current input nodes to activate a second parasitic BJT by current flowing through a first parasitic BJT and

one of the resistors coupled thereto during an ESD event.

16. The ESD protection circuit as claimed in claim 15, wherein each of the resistors is formed by a well of the second conductivity between the first doping region and a fourth doping region coupled to the power line.

17. The ESD protection circuit as claimed in claim 15, wherein a field oxide is disposed between the first and fourth doping region to increase a resistance of the well.

18. The ESD protection circuit as claimed in claim 15, wherein a field oxide is disposed between the second and third doping region isolating one region from the other.

19. The ESD protection circuit as claimed in claim 15, wherein a dummy gate is disposed between the second and third doping region isolating one region from the other.